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Lab Report no: **1**

**LAB REPORT OF Xilinx Vivado Design Suite and Nexys 4 Artix-7 FPGA board**

OBJECTIVE:

This lab is an introduction about how to design, implement and demonstrate a half adder using the Xilinx Vivado Design Suite on the Nexys 4 Artix-7 FPGA board

CODE:

entity lab1\_1 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

S : out STD\_LOGIC;

C : out STD\_LOGIC);

end lab1\_1;

architecture Behavioral of lab1\_1 is

begin

S <= A XOR B;

C <= A AND B;

end Behavioral;

OPERATION:

The main goal of this lab is to add two bits. There are two main operations, XOR operation and AND operation. For the XOR operation, if only one inputs is high, then the output will be high. Otherwise, the output will be low. For the AND operation, only if both two inputs are high, the output will be high.

RESULT:

After implementing the project and setting up the board, I observed the result from the LED light on the board. When I turned on both sw0 and sw1, then all the inputs were high, and LED0 lightened. In other cases, LED0 had no change. It meant the AND operation worked well. Next, while only either sw0 or sw1 was turning on, LED1 lightened. From my observation, the half adder on Nexys 4 board using Xilinx Vivado was implemented successfully.